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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,565	10/31/2005	Edward Fuergut	I431.126.101/FIN 481 PCT/	9154
25281	7590	09/22/2008	EXAMINER	
DICKE, BILLIG & CZAJA FIFTH STREET TOWERS 100 SOUTH FIFTH STREET, SUITE 2250 MINNEAPOLIS, MN 55402			INGHAM, JOHN C	
			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/529,565	Applicant(s) FUERGUT ET AL.	
	Examiner JOHN C. INGHAM	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 10-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-18 is/are allowed.
- 6) ☒ Claim(s) 10-14 and 19-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 March 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The amendments filed 16 June 2008 have been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims **10-14 and 19-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman (US 6,737,750), Ma (US 6,271,469) and Yang (US 6,730,544).
4. Regarding claims **10 and 19-21**, Hoffman discloses in Fig 6A an electronic component comprising: a stack of semiconductor chips having a first semiconductor chip (12) and a stacked second semiconductor chip (16), the semiconductor chips having an active first face (12A, 16A) with contact pads (12C, 16C) to integrated circuits and a second face (12B, 16B); a flat conductor structure (14) having a chip island (14i), flat conductors (horizontal portions of 14k) surrounding the chip island, and contact pillars (vertical portions of 14k) arranged on the flat conductors and aligned orthogonally with respect to the flat conductors; wherein the second semiconductor chip (16) is arranged with its second face (16B) on the chip island and wherein its contact pads (16C) are electrically connected via bonding wire connections (20) to the flat conductors; wherein the first semiconductor chip (12) is surrounded by the contact

pillars (vertical portions of 14K) and is arranged underneath the chip island (14i) such that pillar contact pads (14M) of the contact pillars, first face areas (face of 19 touching 10) of a plastic encapsulation compound (19) that embeds the semiconductor chips, the contact pillars and the flat conductor structure, and the active first face (can be connected in a flip-chip manner, col 4 ln 26-30) of the first semiconductor chip (12A), form an overall first face (10a), and wherein a wiring layer (10, 11A) is arranged on the overall upper face and electrically connects the semiconductor chips to one another via wiring lines (col 7 ln 14-15 and col 10 ln 8-10).

5. Hoffman does not specify that the first face area of the plastic encapsulation and the active first face of the first chip form an overall first face as described in the arguments and specification (the active face of the die and the surface of the encapsulant are planar), although Fig 6A does show a planar interface between items 19 and 10. Ma teaches formation of an encapsulation material for dice that is planar with the active surface of the die in order to increase surface area for trace formation (col 4 ln 1-5). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Ma on the device of Hoffman in order to increase surface area for trace formation.

6. Hoffman and Ma do not specify that the flat conductors extend to edge faces of the plastic encapsulation compound. Instead Hoffman shows in fig 6A that the flat conductors (14k) are within the plastic encapsulation compound. However, Yang teaches that heat can travel through wires and be dissipated to the outside environment through flat conductors extending to edge faces of the encapsulation (col 4 ln 40-44). It

would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Yang on the device of Hoffman and Ma, extending the flat conductors to edge faces of the encapsulation compound, in order to dissipate heat to the outside environment.

7. With regards to claims **11-12 and 22-23**, Hoffman discloses in Fig 6A the component of claim 10, wherein the wiring layer (10) comprises a wiring level (11A) arranged on the overall first face (10A) and comprises outer contact pads (11B) that are electrically connected via the wiring lines (11A) to the pillar contact pads (14M) of the contact pillars (vertical portions of 14K) and to the contact pads (12C) on the first semiconductor chip, and wherein solder balls (15) are arranged on the outer contact pads (11B).

8. With regards to claims **13-14 and 24-25**, Hoffman discloses in Fig 15 the component of claim 10 configured within a panel comprising a leadframe (col 5 ln 40-45) with additional electronic components arranged in rows and columns (col 12 ln 1-5) wherein the shape of the panel corresponds in its extent and extent markings to a standard semiconductor wafer (col 13 ln 8-15).

9. Claims **26 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman, Ma and Yang as applied to claim 11 above, and further in view of Rokugawa (US 6,418,615). Hoffman, Ma and Yang do not specify wherein the wiring layer further comprises an insulation layer situated between the overall first face and the wiring level, the insulation layer having through contacts that electrically connect the

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outer contact pads to the pillar contact pads of the contact pillars and/or to the contact pads on the first semiconductor chip. Hoffman, Ma and Yang also do not specify wherein the wiring layer further comprises a solder resist layer is arranged on the wiring level, the solder resist layer having openings that leave the outer contact pads 20 free.

10. Rokugawa teaches in Fig 1 wherein a wiring layer comprises an insulation layer (14) situated between the overall first face and the wiring level (12) with through contacts (20) electrically connecting outer contact pads (24) to inner contact pads (20A) and a solder resist layer (26) having openings that leave the outer contact pads free, so that the face for mounting the semiconductor elements is as flat as possible (col 2 ln 64 through col 3 ln 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Rokugawa in order to provide a face for mounting the semiconductor elements as flat as possible.

Allowable Subject Matter

11. Claims **15-18** are allowed.

12. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not disclose the limitations of the method of claim 15, wherein the flat conductors extend between neighboring chip islands.

Response to Arguments

13. Applicant's arguments filed 26 June 2007 have been fully considered but they are not persuasive.

14. Regarding the argument on page 7, Ma teaches formation of an encapsulation material for dice that is planar with the active surface of the die in order to increase surface area for trace formation. Although Hoffman teaches a substrate that would have the same advantage, the combination with Ma would be obvious to one of ordinary skill in the art since it further improves the component.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN C. INGHAM whose telephone number is (571)272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Howard Weiss/
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